VLSI PROJECT LIST (VHDL/Verilog)

S.No.	PROJECT TITLES
1	A New VLSI Architecture of Parallel Multiplier–Accumulator Based on Radix-2 Modified Booth Algorithm.
2	An Efficient Architecture for 3-D Discrete Wavelet Transform.
3	The Design of FIR Filter Base on Improved DA Algorithm and its FPGA Implementation.
4	Design of On-Chip Bus with OCP Interface.
5	Design of a Self-Motivated Arbitration Scheme for the Multilayer AHB Busmatrix.
6	Low Complexity and Fast Computation for Recursive MDCT and IMDCT Algorithms
7	A Robust UART Architecture Based on Recursive Running Sum Filter for Better Noise Performance
8	Single chip encryptor/ decryptor core implementation using AES algoritham
9	Implementation of IEEE 802.11 a WLAN Baseband Processor
10	Design of Simple Spectrum Analyzer
11	A Dual-Purpose Real/Complex Logarithmic Number System ALU
12	An Efficient Architecture for 2-D Lifting-based Discrete Wavelet Transform.
13	Power-Efficient Pipelined Reconfigurable Fixed-Width Baugh-Wooley Multipliers
14	A Spurious-Power Suppression Technique for Multimedia/DSP Applications
15	Design of AES (Advanced Encryption Standard) Encryption and Decryption Algorithm with 128-bits Key Length
16	DDR3 based lookup circuit for high-performance network processing.
17	Multiplication Acceleration Through Twin Precision
18	32-bit RISC CPU Based on MIPS
19	High Speed Hardware Implementation of 1D DCT/IDCT
20	Efficient FPGA implementation of convolution
21	High Speed VLSI Architecture for General Linear Feedback Shift Register (LFSR) Structures
22	Implementation of a visible Watermarking in a secure still digital Camera using VLSI design
23	Implementation of FFT/IFFT Blocks for OFDM
24	Design and Synthesis of High speed CAM using Xilinx Spartan3E

25	Embedded a low area 32 bit AES for image encryption and decryption application
26	Implementation of a visible water marking in a secure still digital camera using VLSI design
27	Design and Implementation of a 64-bit RISC Processor using VHDL
28	Design and Implementation of Wi-Fi MAC Transmit Protocol using VHDL
29	High speed parallel architecture for cyclic convolution based on FNT
30	A ParalleYPipelined Algorithm for the Computation of MDCT and IMDCT
31	Integrated Design of AES (Advanced Encryption Standard) Encrypter and Decrypter
32	A Memory-efficient Huffman Decoding Algorithm
33	Minimization of Switching Activities of Partial Products for Designing Low-Power Multipliers
34	A New High-Speed Architecture for Reed-Solomon Decoder
35	Design and Implementation of Efficient Systolic Array Architecture for DWT (Discrete Wavelet Transform)
36	Design and Implementation of 10/100 Mbps (Mega bits per second) Ethernet Switch for Network applications (Verilog)
37	Design and Implementation of USB 2.0 Transceiver Macro-cell Interface (UTMI) (VHDL)
38	Advanced Design Verification methods using VHDL code modification
39	Design and Implementation of Bloom filter using Xilinx ISE
40	A Reusable Distributed Arithmetic Architecture for FIR Filtering
41	Effective Uses of FPGAs for Brute-ForceAttack on RC4 Ciphers USING VHDL
42	Design and synthesis of vhdl Based Cost-Efficient SHA Hardware Accelerators
43	AMBA AHB Bus Protocol Checker with Efficient Debugging Mechanism
44	Asynchronous Computing in Sense Amplifier-based Pass Transistor Logic
45	FPGA implementation of Extended Tiny Encryption Algorithm (XTEA) for Pervasive
46	Low-Power Mixed-Signal CVNS-Based 64-Bit Adder for Media Signal Processing
47	Implementation of a Multi-channel UART Controller Based on FIFO Technique and FPGA
48	IMPLEMENTATION OF A FFT/IFFT MODULE ON FPGA: COMPARISON OF

	METHODOLOGIES
49	A Versatile Multimedia Functional Unit Design Using the Spurious Power Suppression Technique (Verilog)
50	Design and Implementation of Digital low power base band processor for RFID Tags (Verilog)
51	Design and Implementation of Reversible Watermarking for JPEG2000 Standard
52	FPGA Implementation of 3D Discrete Wavelet Transform for Real-Time Medical Imaging
53	Design and Implementation of High Speed DDR SDRAM (Dual Data Rate Synchronously Dynamic RAM) Controller (VHDL)
54	Design and Implementation of Lossless DWT/IDWT for Medical Images
55	High Performance Complex Number Multiplier Using Booth-Wallace Algorithm
56	High Speed Parallel CRC Implementation Based On Unfolding, Pipelining and Retiming
57	A HIGH PERFORMANCE VLSI FFT ARCHITECTURE
58	Design of an Bus Bridge between OCP and AHB Protocol (VHDL)
59	Design of Gigabit Ethernet MAC (Medium Access Control) Transmitter
60	Design of an AMBA-Advanced High performance Bus (AHB) Protocol IP Block
61	Design of Data Encryption Standard (DES)
62	Design of Distributed Arithmetic FIR Filter
63	Design of Universal Asynchronous Receiver Transmitter (UART)
64	Design of Triple Data Encryption Standard (DES)
65	Design of 16 Point Radix-4 FFT (Fast Fourier Transform) Algorithm
66	Design of Dual Elevator Controller
67	Design of an ATM (Automated Teller Machine) Controller
68	Design of 8-Bit Pico Processor

69	Design of JPEG Image compression standard
70	Design of Digital FM Receiver using PLL (Phase Locked Loop)
71	Design of 16-bit QPSK (Quadrature Phase Shift Keying)
72	Design of 16-bit QAM (Quadrature Amplitude Modulation) Modulator
73	Design of AES (Advanced Encryption Standard) Encryption Algorithm with 128-bits Key Length
74	Design of RS-232 System Controller
75	Design of Floating-Point Multiplier using IEEE-754 Standard
76	Design of CRC (Cyclic Redundancy Check) Generator
77	Design and Implementation of OFDM Transmitter
78	Design of 8-bit Microcontroller
79	Design and synthesis of ALU, Verification using Advanced design Verification Technique
80	Design Synthesis and Verification of Simple All Digital FM Receiver using Xilinx FPGA
81	Design, simulation and Synthesis of CPU 8086 using Xilinx FPGA
82	Design and Verification of PCI-Express Bus
83	Design of UART Simulation and Synthesis using Xilinx FPGA
84	Design and Verification of 8 bit Hamming Encoder and Decoder.
85	Design and Verification of Modified Booths Algorithm-Synthesis using Xilinx ISE
86	5x4Gbps 0.35 Micron CMOS CRC Generator Designed With Standard Cells
87	Design and Verification of CACHE COHERENCE MEMORY.
88	Design and Synthesis of MICRO UART using Xilinx spartan3E
89	IMPLEMENTATION OF ETHERNET TRIMODE MAC
90	Design Synthesis and Verification of PCI EXPRESS using Xilinx FPGA

91	Design and Verification of ADAPTIVE FILTER
92	Design and Synthesis of DIGITAL INSTANTANEOUS FREQUENCY MEASUREMENT PROCESSOR
93	Low Power Register Exchange Viterbi Decoder For Wireless Applications
94	PPI - Programmable Peripheral Interface
95	Triple –DES Encryption and Decryption core using
96	Design and Verification of Bluetooth Base Band Controller.
97	Implementation of frame synchronizer using verilog
98	. Design and Synthesis of DIGITAL INSTANTANEOUS FREQUENCY MEASUREMENT PROCESSOR
99	Design and Verification of " IMPROVING MULTIPLIER DESIGN BY USING IMPROVED COLUMN COMPRESSION TREE AND OPTIMIZED FINAL ADDER IN CMOS TECHNOLOGY
100	Double Precision Floating Point Core