Sno	Projects List	IEEE
1	High - Throughput Finite Field Multipliers Using Redundant Basis For FPGA And ASIC Implementations	2015
2	A Generalized Algorithm And Reconfigurable Architecture For Efficient And Scalable Orthogonal Approximation Of Dct	2015
3	Low Delay Single Symbol Error Correction Codes Based On Reed Solomon Codes	2015
4	Fully Reused VLSI Architecture Of Fm0/Manchester Encoding Using Sols Technique For Dsrc Applications	2015
5	Obfuscating Dsp Circuits Via High-Level Transformations	2015
6	Pre-Encoded Multipliers Based On Non-Redundant Radix-4 Signed-Digit Encoding	2015
7	An Efficient Constant Multiplier Architecture Based On Vertical-Horizontal Binary Common Sub-Expression Elimination Algorithm For Reconfigurable Fir Filter Synthesis	2015
8	Flexible Dsp Accelerator Architecture Exploiting Carry-Save Arithmetic	2015
9	Low-Latency High-Throughput Systolic Multipliers Over For Nist Recommended Pentanomials	2015
10	A Synergetic Use Of Bloom Filters For Error Detection And Correction	2015
11	Reliable Low-Power Multiplier Design Using Fixed-Width Replica Redundancy Block	2015

12	Recursive Approach To The Design Of A Parallel Self-Timed Adder	2015
13	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	2015
14	Efficient Sub Quadratic Space Complexity Architectures For Parallel Mpb Single- And Double-Multiplications For All Trinomials Using Toeplitz Matrix-Vector Product Decomposition	2015
15	Fine-Grained Critical Path Analysis And Optimization For Area-Time Efficient Realization Of Multiple Constant Multiplications	2015
16	Fast Sign Detection Algorithm For The Rns Moduli Set {2n+1 - 1, 2n - 1, 2n}	2015
17	Algorithm And Architecture For A Low-Power Content-Addressable Memory Based On Sparse Clustered Networks	2015
18	Scan Test Bandwidth Management For Ultralarge-Scale System-On-Chip Architectures	2015
19	Novel Shared Multiplier Scheduling Scheme For Area-Efficient FFT/IFFT Processors	2015
20	VLSI Computational Architectures For The Arithmetic Cosine Transform	2015
21	A Generalization Of Addition Chains And Fast Inversions In Binary Fields	2015
22	Low-Power And Area-Efficient Shift Register Using Pulsed Latches	2015
23	Communication Optimization Of Iterative Sparse Matrix - Vector Multiply On GPUs And FPGAs	2015

24	A Self-Powered High-Efficiency Rectifier With Automatic Resetting Of Transducer Capacitance In Piezoelectric Energy Harvesting Systems	2015
25	Low-Power Programmable PRPG With Test Compression Capabilities	2015
26	One Minimum Only Trellis Decoder For Non – Binary Low - Density Parity - Check Codes	2015
27	A Low Complexity Scaling Method For The Lanczos Kernel In Fixed-Point Arithmetic	2015
28	Mixing Drivers In Clock-Tree For Power Supply Noise Reduction	2015
29	A Closed-Loop Reconfigurable Switched-Capacitor DC-DC Converter For Sub-mW Energy Harvesting Applications	2015
30	Simplified Trellis Min–Max Decoder Architecture For Nonbinary Low-Density Parity-Check Codes	2015
31	New Regular Radix-8 Scheme For Elliptic Curve Scalar Multiplication Without Pre-Computation	2015
32	Fault Tolerant Parallel Filters Based On Error Correction Codes	2015
33	Comments On "Low-Latency Digit-Serial Systolic Double Basis Multiplier Over GF (2m) Using Subquadrat Ic Toeplitz Matrix-Vector Product Approach"	2015
34	Skewed-Load Test Cubes Based On Functional Broadside Tests For A Low-Power Test Set	2015
35	Low-Complexity Tree Architecture For Finding The First Two	2015

	Minima	
36	Efficient Coding Schemes For Fault-Tolerant Parallel Filters	2015
37	Piecewise-Functional Broadside Tests Based On Reachable States	2015
38	A Multicycle Test Set Based On A Two-Cycle Test Set With Constant Primary Input Vectors	2015
39	Partially Parallel Encoder Architecture For Long Polar Codes	2015
40	Novel Block-Formulation And Area-Delay - Efficient Reconfigurable Interpolation Filter Architecture Formulti - Standard SDR Applications	2015
41	An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator	2014
42	Data Encoding Techniques for Reducing Energy Consumption in Network-on-Chip	2014
43	A Methodology for Optimized Design of Secure Differential Logic Gates for DPA Resistant Circuits	2014
44	Fast Radix-10 Multiplication Using Redundant BCD Codes	2014
45	A parallel radix-sort-based VLSI architecture for finding the first W maximum/minimum values	2014
46	Multifunction Residue Architectures for Cryptography	2014
47	Area-Delay-Power Efficient Fixed-Point LMS Adaptive Filter With Low Adaptation-Delay	2014
48	32 Bit×32 Bit Multiprecision Razor-Based Dynamic Voltage	2014

	Scaling Multiplier With Operands Scheduler	
49	Recursive Approach to the Design of a Parallel Self-Timed Adder	2014
50	Fully Reused VLSI Architecture of FM0/Manchester Encoding Using SOLS Technique for DSRC Applications	2014
51	Statistical Analysis of MUX-Based Physical Unclonable Functions	2014
52	Low-Power Pulse-Triggered Flip-Flop Design Based on a Signal Feed-Through Scheme	2014
53	Bit-Level Optimization of Adder-Trees for Multiple Constant Multiplications for Efficient FIR Filter Implementation	2014
54	Efficient Integer DCT Architectures for HEVC	2014
55	Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm	2014
56	A Method to Extend Orthogonal Latin Square Codes	2014
57	Efficient FPGA and ASIC Realizations of a DA-Based Reconfigurable FIR Digital Filter	2014
58	Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator	2014
59	On the Systematic Creation of Faithfully Rounded Truncated Multipliers and Arrays	2014
60	Design of Efficient Binary Comparators in Quantum-Dot Cellular Automata	2014
61	Low-Latency Successive-Cancellation Polar Decoder Architectures	2014

	Using 2-Bit Decoding	
62	Aging-Aware Reliable Multiplier Design With Adaptive Hold Logic	2014
63	Low-Complexity Low-Latency Architecture for Matching of Data Encoded With Hard Systematic Error-Correcting Codes	2014
64	Area–Delay–Power Efficient Carry-Select Adder	2014
65	Restoration-Based Procedures With Set Covering Heuristics for Static Test Compaction of Functional Test Sequences	2014
66	Scalable Montgomery Modular Multiplication Architecture with Low-Latency and Low-Memory Bandwidth Requirement	2014
67	Digitally Controlled Pulse Width Modulator for On-Chip Power Management	2014
68	Input Test Data Volume Reduction for Skewed-Load Tests by Additional Shifting of Scan-In States	2014
69	Area-Delay Efficient Binary Adders in QCA	2014
70	Sharing Logic for Built-In Generation of Functional Broadside Tests	2014
71	Novel High Speed Vedic Mathematics Multiplier using compressors	2013
72	Design of High Performance 64 bit MAC Unit	2013
73	An FPGA Based High Speed IEEE-754 Double Precision Floating Point Multiplier	2013
74	Error Detection in Majority Logic Decoding of Euclidean Geometry	2013

	Low Density Parity Check(EG-LDPC)codes	
75	Techniques for Compensating Memory Errors in JPEG2000	2013
76	MDC FFT/IFFT Processor With Variable Length for MIMO-OFDM Systems	2013
77	Achieving Reduced Area By Multi-Bit Flip Flop Design	2013
78	Design of Digital-Serial FIR Filters: Algorithms, Architecture and a CAD Tool	2013
79	VLSI implementation of Fast Addition using Quaternary Signed Digit Number System	2013
80	A low power single phase clock distribution using VLSI technology	2013